Amendments to the Specification:

Please replace paragraph [0017] with the following replacement paragraph:

[0017] Figure 1 is a simplified top-down schematic diagram of a standard cell integrated circuit in accordance with one embodiment.

Please replace paragraph [0025] with the following replacement paragraph:

[0025] In one embodiment, ~~the~~ fault ~~detection~~detector circuit 5 is added to the circuit to be monitored (in this case, a microcontroller) using the same computer-aided design (CAD) tool used to design and layout the circuit being monitored. Each of the fault detectors has the same circuitry. This circuitry is described in connection with fault detector 6.

Please replace paragraphs [0031] and [0032] with the following replacement paragraphs:

[0031] The same conditions apply to the circuitry of all the other fault detectors (not shown) of ~~the~~ fault detector circuit 5 that supply signals onto the other input leads 18-24 of logic tree 7. As long as integrated circuit 1 continues to be supplied with a supply voltage Vcc that stays within the normal operating supply voltage range,

each of the fault detectors should continue to output a digital logic high onto its respective input lead to the logic tree 7. The fault signal FAULT supplied onto the input lead 25 of the VBO/POR circuit 3 should therefore remain at a digital logic low.

[0032] In one embodiment, VBO/POR circuit 3 monitors the supply voltage Vcc by detecting the voltage difference between VCC input lead 27 and GND input lead 28. If VBO/POR ~~circuit~~circuit 3 detects the voltage between input leads 27 and 28 to have fallen below a predetermined voltage, then VBO/POR circuit 3 outputs a "voltage brownout" VBO signal on output lead 29 and outputs the active low reset signals PONR1B and PONR2B as set forth above. These active low reset signals PONR1B and PONR2B will cause some of the sequential logic elements of the circuit being monitored to be initialized to predetermined desired values. In the case where the circuit being monitored is a microcontroller, the program counter of the microcontroller is initialized to a known starting value.

Please replace paragraph [0043] with the following replacement paragraph:

[0043] Although the present invention has been described in connection with certain specific embodiments for instructional purposes, the present invention is not limited thereto. The reset circuit of the fault detector circuit need not in all embodiments be a power-on reset circuit. Although a fault detector of fault detector circuit 5 is described above in connection with the

particular fault detector of Figure 2, other types of fault detectors can be employed in fault detector system 5. A sequential logic element such as a memory cell can be used to store a digital logic value whose state can be changed by an EFT event. Transistors and analog circuit components not ordinarily employed in the digital logic circuitry of the circuit being monitored can be used in the fault detectors. The fault detector circuit can be employed to detect faults at the circuit board level. Fault detectors can, for example, be spread across the various discrete integrated circuits on a printed circuit board or other system, and the outputs of the various fault detectors can supplied by a logic tree to a single reset circuit. The various fault detectors of a fault detector system need not all be identical but rather can be different types of circuits designed to detect different types of transient conditions. Multiple fault detectors and an associated logic tree can be implemented without the output of the logic tree being coupled to a reset circuit.